REMARKS

This Amendment responds to the Final Office Action mailed June 15, 2004 in the above-identified application. An RCE is being filed with this Amendment. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-45 are pending in the application. Claims 8-29 and 43-45 have been withdrawn from consideration. Claims 1, 6, 30, 34, 35, 36, 39 and 41 have been amended. Claims 2, 3, 7, 31, 37, 38, 40 and 42 have been cancelled without prejudice or disclaimer. As a result, claims 1, 4-6, 30, 32-36, 39 and 41 are pending for examination, with claims 1, 6, 30, 34, 36 and 41 being independent claims. No new matter has been added.

The Examiner has rejected claims 1-3, 6-7, 30-31, 34-35 and 41-42 under 35 U.S.C. §102(e) as anticipated by Cypher (U.S. 6,289,420). Claims 4-5 and 32-33 are rejected under 35 U.S.C. §103(a) as unpatentable over Cypher in view of Malamy et al. (U.S. 5,675,765). Claims 36-40 are rejected under 35 U.S.C. §103(a) as unpatentable over Cypher in view of Sager et al. (U.S. 6,425,055). The rejections are respectfully traversed.

Cypher discloses a cache memory that includes a plurality of memory chips which are configured to collectively store a plurality of cache lines. Each cache line includes data and an associated cache tag (Abstract). Each cache line is stored across the memory chips in a row formed by corresponding entries accessed using the same index address (Abstract; Fig. 2 and col. 4, lines 49-65). The plurality of cache lines is grouped into separate subsets based on index addresses, thereby forming several separate classes of cache lines. The cache tags associated with cache lines of different classes are stored in different memory chips (Abstract; Fig. 3 and col. 5, lines 8-26). During operation the cache controller may receive multiple snoop requests corresponding to transactions initiated by various processors. The cache controller is configured to concurrently access the cache tags of multiple lines in response to the snoop requests if the lines correspond to differing classes (Abstract). The Cypher patent does not disclose a cache memory having two or more ways.

Amended claim 1 is directed to a cache memory system comprising a plurality of memory locations for storing data and addresses associated with the data, wherein the memory locations are organized as two or more ways, and at least one controller that enables a first device to access a first way selected from the two or more ways and enables a second device to

access a second way selected from the two or more ways, wherein the first device can access any location in the first way and the second device is blocked from accessing the first way during access by the first device, wherein the second device can access any location in the second way and the first device is blocked from accessing the second way during access by the second device, and wherein the first and second ways can be accessed concurrently by the first and second devices, respectively.

The cache memory defined by amended claim 1 is very different from the cache memory disclosed by Cypher. Cypher permits concurrent access to different classes of cache lines. As shown in Figs. 2 and 3 of Cypher, different classes correspond to different index addresses. Cypher does not disclose or suggest a cache memory *wherein a first device accesses a first way selected from two or more ways and a second device accesses a second way selected from the two or more ways, wherein the first device can access any location in the first and the second device is blocked from accessing the first way during access by the first device, wherein the second device can access any location in the second way and the first device is blocked from accessing the second way during access by the second device, and wherein the first and second ways can be accessed concurrently by the first and second devices, respectively,* as required by amended claim 1. Cypher contains no disclosure of a cache memory having first and second ways but instead discloses concurrent access to different classes of cache lines. The above limitations are not disclosed or even remotely suggested by Cypher. Accordingly, amended claim 1 is clearly and patentably distinguished over Cypher, and withdrawal of the rejection is respectfully requested.

Claims 4 and 5 depend from claim 1 and are patentable over Cypher for at least the reasons discussed above in connection with claim 1.

Amended claim 6 is directed to a cache memory system comprising a plurality of memory locations to store data and addresses associated with the data, wherein the memory locations are organized as two or more ways, a plurality of cache outputs for providing data retrieved from the memory locations, and first and second multiplexers having inputs coupled to at least some of the memory locations and outputs coupled to the plurality of cache outputs so as to enable the first multiplexer to select data from a first way selected from two or more ways and to enable the second multiplexer to select data from a second way selected from the two or more ways, wherein the first multiplexer can select data from any location in the first way and the

second multiplexer can select data from any location in the second way, and wherein the selected data from the first and seconds ways is provided concurrently on respective ones of the plurality of cache outputs.

Cypher does not disclose or suggest a cache memory system including *first and second multiplexers having inputs coupled to memory locations and outputs coupled to cache outputs to enable the first multiplexer to select data from a first way selected from two or more ways and to enable the second multiplexer to select data from a second way selected from the two or more ways, wherein the first multiplexer can select data from any location in the first way and the second multiplexer can select data from any location in the second way, and wherein the selected data from the first and second ways is provided concurrently on respective ones of the plurality of cache outputs,* as required by amended claim 6. Cypher discloses no multiplexers of any type. Further, Cypher does not disclose or suggest selecting data from first and second ways and providing the selected data from the first and second ways concurrently on respective ones of the cache outputs. As noted above, Cypher discloses concurrent access to different classes of cache lines rather than concurrent access to different ways. For these reasons, amended claim 6 is clearly and patentably distinguished over Cypher, and withdrawal of the rejection is respectfully requested.

Amended claim 30 is directed to a method of operating an associative cache having a plurality of memory locations for storing data, wherein the memory locations are organized as two or more ways. The method comprises accessing with a first device a first way selected from the two or more ways and accessing with a second device a second way selected from the two or more ways, wherein the first device can access any location in the first way and the second device is blocked from accessing the first way during access by the first device, wherein the second device can access any location in the second way and the first device is blocked from accessing the second way during access by the second device, and wherein the first and second ways can be accessed concurrently by the first and second devices, respectively.

Amended claim 30 is clearly patentable over Cypher for at least the reasons discussed above in connection with claim 1. In particular, Cypher does not disclose or suggest concurrently accessing first and second ways, wherein the first and second ways are accessed concurrently by first and second devices, respectively, and wherein any location in the respective ways can be accessed. Cypher discloses concurrent access to different classes of cache lines

rather than concurrent access to different ways. For these reasons, amended claim 30 is clearly and patentably distinguished over Cypher, and withdrawal of the rejection is respectfully requested.

Claims 32 and 33 and depend from claim 30 and are patentable over Cypher for at least the reasons discussed above in connection with claims 1 and 30.

Amended claim 34 is directed to a method of operating an associative cache having a plurality of memory locations for storing data, and a plurality of outputs for providing data retrieved from the memory locations to respective devices. The method comprises concurrently providing data from different locations of the plurality of memory locations to the respective devices via the plurality of outputs, wherein first data from a first way selected from two or more ways is provided to a first device via a first output and second data from a second way selected from the two or more ways is provided to a second device via a second output, wherein the first data can be selected from any location in the first way and the second data can be selected from any location in the second way.

As discussed above in connection with claims 1 and 6, Cypher contains no disclosure or suggestion of concurrently providing data from different locations to respective devices, wherein data from first and second ways is provided to first and second devices, respectively, and wherein the data can be selected from any location in the respective ways. Cypher discloses concurrent access to different classes of cache lines rather than concurrent access to different ways. For these reasons and for the reasons discussed above, amended claim 34 is clearly and patentably distinguished over Cypher, and withdrawal of the rejection is respectfully requested.

Claim 35 depends from claim 34 and is patentable over Cypher for at least the reasons discussed above in connection with claims 1, 6 and 34.

Amended claim 36 is directed to a method of operating an associative cache having a plurality of memory locations, wherein the memory locations are organized as two or more ways. The method comprises using multiple decoders to decode respective addresses provided to the cache, including using a first decoder to decode a first address to access a first way selected from the two or more ways and using a second decoder to decode a second address to access a second way selected from the two or more ways, wherein the first address can access any location in the first way and the second address can access any location in the second way, and wherein the first and second ways can be accessed concurrently by the first and second addresses, respectively.

Cypher contains no disclosure or suggestion of using multiple decoders to decode first and second addresses to access first and second ways, respectively, wherein the first and second addresses are decoded to access the first and second locations concurrently. Cypher discloses concurrent access to different classes of cache lines rather than concurrent access to different ways. Sager does not provide the teachings that are lacking in Cypher. In particular, Sager does not disclose or suggest concurrent access to first and second ways, as claimed. For these reasons, amended claim 36 is clearly and patentably distinguished over Cypher in view of Sager, and withdrawal of the rejection is respectfully requested.

Claim 39 depends from claim 36 and is patentable over Cypher in view of Sager for at least the reasons discussed above in connection with claim 36.

Amended claim 41 is directed to a cache memory system comprising a plurality of memory locations for storing data and addresses associated with the data, wherein the memory locations are organized as two or more ways, and means for enabling a first device to access a first way selected from the two or more ways and enabling a second device to access a second way selected from the two or more ways, wherein the first device can access any location in the first way and the second device is blocked from accessing the first way during access by the first device, wherein the second device can access any location in the second way and the first device is blocked from accessing the second way during access by the second device, and wherein the first and second ways can be accessed concurrently by the first and second devices, respectively.

Amended claim 41 is clearly patentable over Cypher for at least the reasons discussed above in connection with claim 1. Accordingly, withdrawal of the rejection of claim 41 is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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